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10/709,362	04/29/2004	David J. Hathaway	BUR920040074US1	3361

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EXAMINER	
LE, TOAN M	
ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 10/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No. 10/709,362	Applicant(s) HATHAWAY ET AL.	
	Examiner Toan M. Le	Art Unit 2863	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,12-22 and 25-31* is/are rejected.

7)☒ Claim(s) *10,11,23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-9, 12-22, and 25-31 are rejected under 35 U.S.C. 102(a) as being anticipated by "Blocked-Based Static Timing Analysis with Uncertainty", Devgan et al. (referred hereafter Devgan et al.).

Referring to claims 1 and 14, Devgan et al. disclose a method and a computer-readable medium containing instructions that, when executed, cause a computer analyzing the timing of a circuit (Abstract), comprising:

determining at least one location information for one or more inputs to a timing test (pages 608-610, entire section 2; figure 1); and

computing a timing slack variation for the timing test using the at least one location information; and

one of:

design the circuit based on the analysis of the timing; and

identifying the cause of timing failures in an existing circuit (pages 607-608, Introduction section),

wherein the one or more inputs comprise cells or elements of interest, and

wherein the method presicts a delay in circuit paths by considering a portion of the delay that is influenced by a proximity of circuit elements in a path or paths separately from a full delay distribution (page 610, 1st col., lines 6-17; pages 610-612, entire section 3; figure 9).

As to claims 2 and 15, Devgan et al. disclose a method and a computer-readable medium containing instructions that, when executed, cause a computer analyzing the timing of a circuit (Abstract), wherein the input to a timing test is a path or a logic cone (figures 8-9).

Referring to claims 3 and 16, Devgan et al. disclose a method and a computer-readable medium containing instructions that, when executed, cause a computer analyzing the timing of a circuit (Abstract), wherein the at least one location information comprises a bounding region for the one or more inputs to the timing test (page 609, 2nd col., Max operation section; page 610, section 2.1; figure 5).

As to claims 4 and 17, Devgan et al. disclose a method and a computer-readable medium containing instructions that, when executed, cause a computer analyzing the timing of a circuit (Abstract), wherein said determining comprises defining the bounding region based an the locations of the one or more inputs to the timing test (page 609, 2nd col., Max operation section; page 610, section 2.1; figure 5).

Referring to claims 5 and 18, Devgan et al. disclose a method and a computer-readable medium containing instructions that, when executed, cause a computer analyzing the timing of a circuit (Abstract), wherein said determining further comprises modifying a. size of the bounding region to account for variations in delay among the one or more inputs to the timing test (page 609, 2nd col., last paragraph; page 610, 1st col., lines 1-5 and section 2.1).

As to claims 6 and 19, Devgan et al. disclose a method and a computer-readable medium containing instructions that, when executed, cause a computer analyzing the timing of a circuit (Abstract), wherein said computing comprises:

determining a slack variation factor based an the size of the bounding region; and

adding the slack variation factor to a timing slack calculated for the one or more inputs to the timing test (page 609, 2nd col., Addition Operation section; page 610, section 2.1).

Referring to claims 7 and 20, Devgan et al. disclose a method and a computer-readable medium containing instructions that, when executed, cause a computer analyzing the timing of a circuit (Abstract), comprising:

determining at least one location information for one or more inputs to a timing test (pages 608-610, entire section 2);

computing a timing slack for the timing test using the at least one location information; and

one of:

designing the circuit based on the analysis of the timing; and

identifying the cause of timing failures in an existing circuit (pages 607-608, Introduction section),

wherein the at least one location information comprises a centroid of the one or more inputs to the timing test (page 610, 1st col., lines 6-17; pages 610-612, entire section 3; figure 9).

As to claims 8 and 21, Devgan et al. disclose a method and a computer-readable medium containing instructions that, when executed, cause a computer analyzing the timing of a circuit

(Abstract), wherein the centroid comprises the averaged location of the one or more inputs to the timing test (figure 9).

Referring to claims 9 and 22, Devgan et al. disclose a method and a computer-readable medium containing instructions that, when executed, cause a computer analyzing the timing of a circuit (Abstract), wherein the centroid comprises the delay-weighted averaged location of the one or more inputs to the timing test (figure 9).

As to claims 12 and 25, Devgan et al. disclose a method and a computer-readable medium containing instructions that, when executed, cause a computer analyzing the timing of a circuit (Abstract), wherein the at least one location information comprises an abstract location information (page 607, 1st col., section 1: 2nd paragraph).

Referring to claims 13 and 26, Devgan et al. disclose a method and a computer-readable medium containing instructions that, when executed, cause a computer analyzing the timing of a circuit (Abstract), wherein the abstract location information is based upon correlation of delay functions (page 610, section 2.1).

As to claim 27, Devgan et al. disclose a method of analyzing the timing of an integrated circuit (Abstract), comprising:

identifying an early path and a late path in the integrated circuit (figures 8-9);

determining a timing slack variation in the early path using location information an one or more elements i n the early path;

determining a timing slack variation in the late path using location information an one or more elements in the late path (pages 608-610, section 2); and

computing a new timing slack for the early path and the late path by using the timing slack variation in the early path and the timing slack variation in the late path (page 610, 1st col., lines 6-17); and

one of:

designing the integrated circuit based on the analysis of the timing; and

identifying the cause of timing failures in an existing circuit (pages 607-608, Introduction section).

Referring to claim 28, Devgan et al. disclose a method of analyzing the timing of an integrated circuit (Abstract), wherein the location information an the one or more elements in the early path and the location information an the one or more elements in the late path comprise bounding regions defined around the one or more elements in the early path and the one or more elements in the late path, respectively (page 609, 2nd col., Max Operation section; page 610, section 2.1).

As to claim 29, Devgan et al. disclose a method of analyzing the timing of an integrated circuit (Abstract), wherein the location information on the one or more elements in the early path and the location information on the one or more elements in the late path comprise centroids calculated by considering the one or more elements in the early path and the one or more elements in the late path, respectively, as aggregates (figure 9).

Referring to claim 30, Devgan et al. disclose a method of analyzing the timing of an integrated circuit (Abstract), wherein the method is performed for an early mode timing analysis of the integrated circuit and a late mode timing analysis of the integrated circuit (page 608, 2nd col., section 2: 1st and last paragraphs).

As to claim 31, Devgan et al. disclose a computer-readable medium containing instructions that, when executed, cause a computer analyzing the timing of a circuit (Abstract), wherein a delay in circuit paths by considering a portion of the delay that is influenced by a proximity of circuit elements in a path or paths separately from a full delay distribution (page 610, 1st col., lines 6-17; pages 610-612, entire section 3).

Allowable Subject Matter

Claims 10-11 and 23-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The reason for allowance of claims 10 and 23 is the inclusion of calculating a first/second centroid of a first/second input to the timing test and determining the distance between the first and second centroids.

The reason for allowance of claims 11 and 24 is the inclusion of determining a slack variation factor based on the distance between the first and second centroids and adding the slack variation factor to a timing slack calculated for the one or more inputs to the timing test.

Response to Arguments

Applicant's arguments with respect to claims 1-31 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments filed 8/3/06 have been fully considered but they are not persuasive.

Referring to claims 1 and 14, Applicant argues that "However, it is not apparent that DEVGAN discloses, or even suggest, that the method predicts a delay in circuit paths by

considering a portion of the delay that is influenced by a proximity of circuit elements in a path or paths separately from a full delay distribution."

Answer: Devgan discloses "In general, an input of a gate may depend on more than one previous mode. For example, in Figure 9, the inputs of the gate 5 depends on A, B, C and D. Some of these vertices may also share subpaths when reaching the inputs of gate 5. Therefore, when computing the arrival time at the output of gate 5, this dependency must be accounted for. To accomplish this, we maintain a Dependency List (DL) with each vertex in the timing graph which lists the vertices on which the arrival time of the current vertex depends.... The DL is propagated as we compute the statistical arrival times using the DLPropagate algorithm shown in Figure 10."

In addition, Figure 9 shows "other logic" for a portion of the delay that is influenced by a proximity of circuit elements in a path or paths separately from a full delay distribution.

Thus, Devgan does teach predicts a delay in circuit paths by considering a portion of the delay that is influenced by a proximity of circuit elements in a path or paths separately from a full delay distribution.

As to claims 7 and 20, Applicant argues that "Furthermore, while the Examiner has identified page 610, col. 1, lines 6-17 and pages 610-612, section 3 and Figure 9 as disclosing that the at least one location information comprises a centroid of the one or more inputs to the timing test (claims 7 and 20), it is apparent that the cited language is silent with regard to utilizing in the analysis a centroid of the one or more inputs to the timing test. Nor has the Examiner explained how such language or the drawing of Figure 9 can be interpreted to disclose or suggest utilizing a centroid of the one or more inputs to the timing test in the analysis"

Answer: Devgan discloses "In general, an input of a gate may depend on more than one previous mode. For example, in Figure 9, the inputs of the gate 5 depends on A, B, C and D. Some of these vertices may also share subpaths when reaching the inputs of gate 5. Therefore, when computing the arrival time at the output of gate 5, this dependency must be accounted for. To accomplish this, we maintain a Dependency List (DL) with each vertex in the timing graph which lists the vertices on which the arrival time of the current vertex depends.... The DL is propagated as we compute the statistical arrival times using the DLPropagate algorithm shown in Figure 10." In addition, Figure 9 shows "other logic" for a centroid of the one or more inputs to the timing test.

Therefore, Devgan does teach at least one location information comprises a centroid of the one or more inputs to the timing test.

Referring to claim 27, Applicant argues that "there is no apparent disclosure or suggestion indicating that both early and late path are accounted for, much less, that a timing slack variation thereof is utilized in the analysis." And that "DEVGAN clearly fails to disclose the logic cone of claims 2 and 15, the bounding region recited in claims 3-6, 16-19 and 28, and abstract location information of claims 12, 13, 25, and 26."

Answer: Devgan discloses in figure 8, "We illustrate the basic principle behind our approach through the circuit in Figure 8. In this examples, two paths originating from node r reconverge as inputs to the same gate at node i and j (logic cone as defined in the Spec. as the entire set of gates which converge on a timing test [0020]). This causes both the arrival time A_i and A_j to depend on arrival time A_r." And "It should be noted that the interdependence of arrival time A_i and A_j has a very specific linear form. That is $A_i = A_r + D_1$ and $A_j = A_r + D_2$. The

variable of interest, arrival time at node o, A_o is given by $A_o = \max(A_r + D_1 + D_{io} + A_r + D_2 + D_{jo})$ (page 611, 1st col., 1st paragraph).

Thus, Devgan does teach an early/late path and timing slack variation and bounding region.

Figure 8 also show "Delay from Node r to Node i through Path 1 and Delay from Node r to Node j through Path 2."

Therefore, Devgan does teach abstract location information.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan M. Le whose telephone number is (571) 272-2276. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Toan Le

October 12, 2006

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